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1. (Amended) A multi-service circuit which receives information-bearing cells on an external interface, the multi-service circuit being controlled by a processor, the multi-service circuit comprising:

plural service devices handling differing telecommunication services;

a multiplexer/demultiplexer core connected between the plural service devices and the external interface, the core having a downstream side for transmitting cells from the external interface to the service devices and an upstream side for transmitting cells from the service devices to the external interface, the upstream side including an upstream multiplexer and an upstream demultiplexer, the downstream side having a downstream demultiplexer and a downstream multiplexer where are distinct from the upstream multiplexer and upstream demultiplexer,

wherein the downstream demultiplexer serves to route cells received from the external interface either:

(1) to an input of the downstream multiplexer; or

(2) to one of:

(a) a downstream loop back buffer which stores cells routed from the downstream side to the upstream side, and

(b) the processor.

2. The apparatus of claim 1, wherein the downstream multiplexer serves to obtain cells from either:

(1) the downstream demultiplexer, or

(2) one of:

(a) an upstream loop-back buffer which stores cells routed from the upstream side to the downstream side, and

(b) the processor,

for transmission to the service devices.

3. The apparatus of claim 2, wherein the downstream demultiplexer and the downstream multiplexer are capable of independent simultaneous operation except when cells are routed from the downstream demultiplexer to the downstream multiplexer.

4. (Amended) The apparatus of claim 1, wherein the upstream side has an upstream demultiplexer and an upstream multiplexer, and

wherein the upstream demultiplexer serves to route cells received from the service devices to one of:

(1) a buffering section situated between the upstream demultiplexer and the upstream multiplexer; and

(2) either:

(a) an upstream loop-back buffer, or

(b) the processor.

5. The apparatus of claim 1, wherein the upstream demultiplexer serves to route cells received from the service devices and from the processor to one of:

(1) the buffering section situated between the upstream demultiplexer and the upstream multiplexer; and

(2) either:

(a) the upstream loop-back buffer, or

(b) the processor.

6. (Amended) The apparatus of claim 4, wherein the upstream multiplexer serves to obtain cells from one of the buffering section and the downstream loop-back buffer, wherein such obtained cells may be sent to the external interface.

7. The apparatus of claim 1, wherein at least one of the service devices is an ATMF transceiver.

8. The apparatus of claim 1, wherein at least one of the service devices is an emulator which interfaces with one of: (1) a PCM interface; (2) a E1 interface; and (3) a T1 interface.

9. The apparatus of claim 8, wherein the emulator has a buffer which is either totally filled or partially filled with data from one channel.

10. The apparatus of claim 8, wherein the emulator has a buffer which is either totally filled or partially filled with data from all channels.

11. The apparatus of claim 1, wherein at least one of the service devices is a Utopia 2 level device.

12. The apparatus of claim 1, wherein the cells are ATM cells.

13. The apparatus of claim 1, wherein a Utopia level 2 tributary interface connects the plural service devices to the multiplexer/demultiplexer core.

14. The apparatus of claim 1, wherein the multi-service circuit is formed as an integrated chip.

15. The apparatus of claim 1, wherein the multi-service circuit is formed entirely by hardware.

16. (Amended) A multi-service circuit which receives information-bearing cells on an external interface, the multi-service circuit being controlled by a processor, the multi-service circuit comprising:

plural service devices handling differing telecommunication services;

a multiplexer/demultiplexer core connected between the plural service devices and the external interface, the core having a downstream side for transmitting cells from the external interface to the service devices and an upstream side for transmitting cells from the service devices to the external interface, the upstream side having an upstream multiplexer and an upstream demultiplexer, and the downstream side including a downstream multiplexer and a downstream demultiplexer,

wherein the upstream demultiplexer serves to route cells received from the service devices to one of:

(1) a buffering section situated between the upstream demultiplexer and the upstream multiplexer; and

(2) either:

(a) an upstream loop-back buffer which routes cells from the upstream side to the downstream side, or

(b) the processor.

17. The apparatus of claim 16, wherein the upstream demultiplexer serves to route cells received from the service devices and from the processor to one of:

(1) the buffering section situated between the upstream demultiplexer and the upstream multiplexer; and

(2) either:

(a) the upstream loop-back buffer, or

(b) the processor.

18. (Amended) The apparatus of claim 17, wherein the upstream multiplexer serves to obtain cells from one of the buffering section and the downstream loop-back buffer, so that such obtained cells may be sent to the external interface.

19. The apparatus of claim 16, wherein at least one of the service devices is an ATMF transceiver.

20. The apparatus of claim 16, wherein at least one of the service devices is an emulator which interfaces with one of: (1) a PCM interface; (2) a E1 interface; and (3) a T1 interface.

21. The apparatus of claim 20, wherein the emulator has a buffer which is either totally filled or partially filled with data from one channel.

22. The apparatus of claim 20, wherein the emulator has a buffer which is either totally filled or partially filled with data from all channels.

23. The apparatus of claim 16, wherein at least one of the service devices is a Utopia 2 level device.

24. The apparatus of claim 16, wherein the cells are ATM cells.

25. The apparatus of claim 16. wherein a Utopia level 2 tributary interface connects the plural service devices to the multiplexer/demultiplexer core.

26. The apparatus of claim 16, wherein the multi-service circuit is formed as an integrated chip.

27. The apparatus of claim 16, wherein the multi-service circuit is formed entirely by hardware.

28. A multi-service circuit which receives ATM cells on an external interface from a modem/transceiver, the multi-service circuit being controlled by a processor, the multi-service circuit comprising:

plural service devices handling differing telecommunication services;

a multiplexer/demultiplexer core connected between the plural service devices and the external interface, the core having:

a downstream side for transmitting cells from the external interface to the service devices and an upstream side for transmitting cells from the service devices to the external interface, the downstream side having a downstream demultiplexer and a downstream multiplexer, the upstream side having an upstream multiplexer and an upstream demultiplexer,

a downstream loop-back buffer for storing cells routed from the downstream side to the upstream side;

an upstream loop-back buffer for storing cells routed from the upstream side to the downstream side;

wherein the downstream demultiplexer serves to route cells received from the external interface to one of the downstream loop back buffer, the processor, and an input of the downstream multiplexer;

wherein the downstream multiplexer serves to obtain cells from one of the downstream demultiplexer, the upstream loop-back buffer, and the processor for transmission to the service devices;

wherein the upstream demultiplexer serves to route cells received from the service devices and from the processor to one of the upstream loop-back buffer, the processor, and a buffering section situated between the upstream demultiplexer and the upstream multiplexer; and

wherein the upstream multiplexer serves to obtain cells from one of the buffering section and the downstream loop-back buffer for application to the external interface.

29. The apparatus of claim 28, wherein the downstream demultiplexer and the downstream multiplexer are capable of independent simultaneous operation except when cells are routed from the downstream demultiplexer to the downstream multiplexer.

30. The apparatus of claim 29, wherein at least one of the service devices is an ATMF transceiver.

31. The apparatus of claim 29, wherein at least one of the service devices is an emulator which interfaces with one of: (1) a PCM interface; (2) a E1 interface; and (3) a T1 interface.

32. The apparatus of claim 31, wherein the emulator has a buffer which is either totally filled or partially filled with data from one channel.

33. The apparatus of claim 31, wherein the emulator has a buffer which is either totally filled or partially filled with data from all channels.

34. The apparatus of claim 29, wherein at least one of the service devices is a Utopia 2 level device.

35. The apparatus of claim 29, wherein the cells are ATM cells.

36. The apparatus of claim 29, a Utopia level 2 tributary interface connects the plural service devices to the multiplexer/demultiplexer core.

37. The apparatus of claim 29, wherein the multi-service circuit is formed as an integrated chip.

38. The apparatus of claim 29, wherein the multi-service circuit is formed entirely by hardware.

39. (Amended) A multi-service circuit which receives ATM cells on an external interface from a modem/transceiver, the multi-service circuit being controlled by a processor, the multi-service circuit being fabricated as a chip and comprising:

plural service devices handling differing telecommunication services;

a multiplexer/demultiplexer core connected between the plural service devices and the external interface, said core including each of a downstream multiplexer, a downstream demultiplexer, an upstream multiplexer and an upstream demultiplexer;

an internal interface connecting the core to the plural service devices; and

wherein, in a downstream direction, the core routes respective cells received from the external interface to: (i) one of the plural service devices via the internal interface, (ii) the processor, and (iii) the external interface;

wherein, in an upstream direction, the core routes cells received from the plural service devices to one of the external interface, to the processor.

40. The apparatus of claim 39, wherein at least one of the external interface and the internal interface are a Utopia level 2 interface.

41. The apparatus of claim 39, wherein the multi-service circuit is formed entirely by hardware.